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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/682,473	09/06/2001	Anthony Richard Bonaccio	BUR920010063	4175

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EXAMINER

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ART UNIT	PAPER NUMBER
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2816

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Please find below and/or attached an Office communication concerning this application or proceeding.



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**BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES**

Paper No. 20040324

Application Number: 09/682,473  
Filing Date: September 06, 2001  
Appellant(s): BONACCIO ET AL.

\_\_\_\_\_  
Brian M. Dugan  
For Appellant

**EXAMINER'S ANSWER**

**MAILED**

MAY 26 2004

**GROUP 2800**

This is in response to the appeal brief filed 12-06-03.

**(1) *Real Party in Interest***

A statement identifying the real party in interest is contained in the brief.

**(2) *Related Appeals and Interferences***

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

**(3) *Status of Claims***

The statement of the status of the claims contained in the brief is correct.

**(4) *Status of Amendments After Final***

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

**(5) *Summary of Invention***

The summary of invention contained in the brief is correct.

**(6) *Issues***

The appellant's statement of the issues in the brief is correct.

**(7) *Grouping of Claims***

The rejection of claims 8 and 13 stand or fall together because appellant's brief does not include a statement that this grouping of claims does not stand or fall together and reasons in support thereof. See 37 CFR 1.192(c)(7).

**(8) *Claims Appealed***

The copy of the appealed claims contained in the Appendix to the brief is correct.

**(9) Prior Art of Record**

6,184,736	Wissell et al	2-2001
5,448,188	Matsumoto et al	9-1995
6,469,547	Rabii	10-2002
5,157,277	Tran et al	10-1992

**(10) Grounds of Rejection**

The following ground(s) of rejection are applicable to the appealed claims:

Claims 8 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Wissell et al reference (U.S. Patent 6,184,736) in view of the Matsumoto et al reference (U. S. Patent 5,448,188).

Wissell discloses in figure 2 an apparatus comprising a generating circuit 42 for generating a differential signal pair (42a and 42b); a distribution circuit (blocks 48 and lines 24) coupled to the generating circuit to distribute the differential signal pair on the IC; a plurality of clock receiver circuits (receiver circuit 32) coupled to the distribution circuit to receive the sinusoidal signal pair as partially required by claim 13. Wissell does not disclose the receiver circuit to output a local clock signal as recited in claim. Matsumoto discloses in figure 1 a receiver circuit for producing a clock output signal by employing both of the sinusoidal signal pair (i.e., generating a *differential* sinusoidal signal pair comprising of a first sinusoidal signal V1 and a second sinusoidal signal V2; and generating a clock signal Vout from the differential pair for the IC by employing both the first and second sinusoidal signals to form the clock signal). It would have been obvious to one skilled in the art at the time the invention was made to

incorporate the teaching of Matsumoto into that of Wissell because a receiver circuit can be implemented in many different ways to accommodate the requirement of particular application. A skilled artisan would have been motivated to combine these references to produce a stabilized clock output signal for a distribution circuit by mixing corresponding a pair of differential sinusoidal signals from a plurality of pairs of differential sinusoidal input signals.

As to claim 8, it is rejected for reciting methods and/or steps derived from the apparatus rejected in claim 13 noted above.

**(11) Response to Argument**

Appellant has argued that "the Wissell et al. reference does not employ both sinusoidal signals received as inputs to the receiver chip shown in FIG. 3 to generate either of the digital clock signals output from the receiver chip of FIG. 3". Examiner does not dispute the above assertion. However, Appellant's argument is irrelevant since the rejection of claims does not rely entirely on the Wissell et al reference to reject "the receiver" limitation. Claims 8 and 13 are rejected under 35 USC 103, in which Wissell et al is used as the primary reference that discloses all the claim limitations except for the details of the receiver as required by claim. The Matsumoto et al reference is a secondary reference that discloses a receiver that converts a differential sinusoidal pair into a clock signal as required by claim. It is the combination of these prior art references that renders the limitation of claims 8 and 13 obvious under 35 USC 103.

Appellant argues that *the specification defines the term 'differential sinusoidal signal pair' as 'a pair of sinusoidal wave forms, that are substantially equal in frequency and amplitude but that are substantially 180° out of phase with each other'; and concludes that this*

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*definition is consistent with the conventional understanding of the term 'differential sinusoidal signal pair'.* Appellant has also pointed out that the sinusoidal signals of Wissell are *90° apart, not 180° apart* and, therefore, concluded that the sinusoidal signals of Wissell are not a differential sinusoidal signal pair.

With respect to the term “differential”, Appellant has argued that a 90° apart signal pair is not a differential signal pair. Examiner respectfully disagrees with Appellant’s position and has addressed this issue in the Final Office Action, dated May 20, 2002, that any pair of signals having significant non-overlapped portions can be considered as being ‘differential’. Only complementary and non-overlapped signals are considered as being 180° apart. Appellant did not challenge Examiner’s position on this issue in subsequent responses. To support Examiner’s position on this issue, the Rabii reference (U.S. Patent 6,469,547) is cited to show that a 90° apart signal pair is known in the art as a differential pair (see col. 3, lines 63-66). Therefore, a pair of differential sinusoidal signals does not need to be 180° apart.

In conclusion, the phrase “differential signals”, using a broad interpretation, is seen generically to refer to any pair of signals having a phase difference with respect to each other, and there is specific terminology in the art to pairs of signals having a phase difference of 90° or 180°, i.e. quadrature and complementary signals, respectively.

Appellant further argues that “the Matsumoto et al. reference has nothing to do with generating a clock signal, as recited in claim 8”. Examiner respectfully disagrees since Matsumoto discloses in figure 1 an apparatus for providing a sine wave Vout that can be clearly interpreted as “a clock signal” as required by the claim. The Tran reference (U.S. Patent


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5,157,277) was cited previously by the Examiner to support this position. Note specifically, figures 1-2 and column 2, lines 52-55, of Tran which clearly disclose that a sine wave is a type of clock signal. Therefore, the teachings of Matsumoto combined with the circuitry of Wissell are seen to obviate the clock limitation of claims 8 and 13.


For the above reasons, it is believed that the rejections should be sustained.


Respectfully submitted,

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May 17, 2004 

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